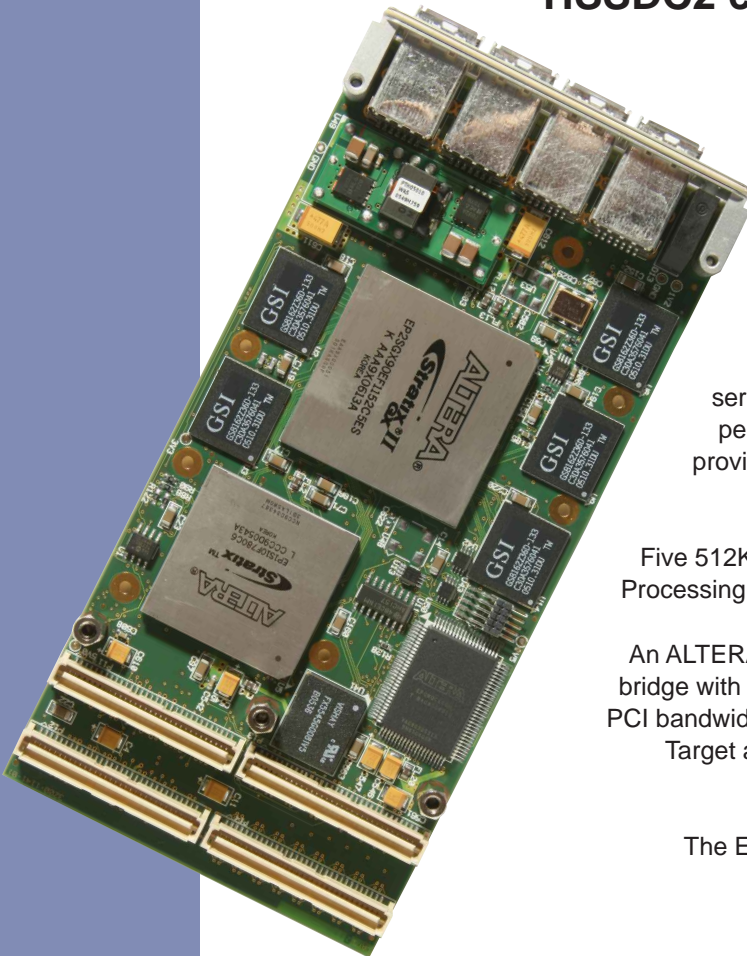


PM432

Stratix II GX FPGA PMC Module with four HSSDC2 connectors and 90Mb ZBT RAM



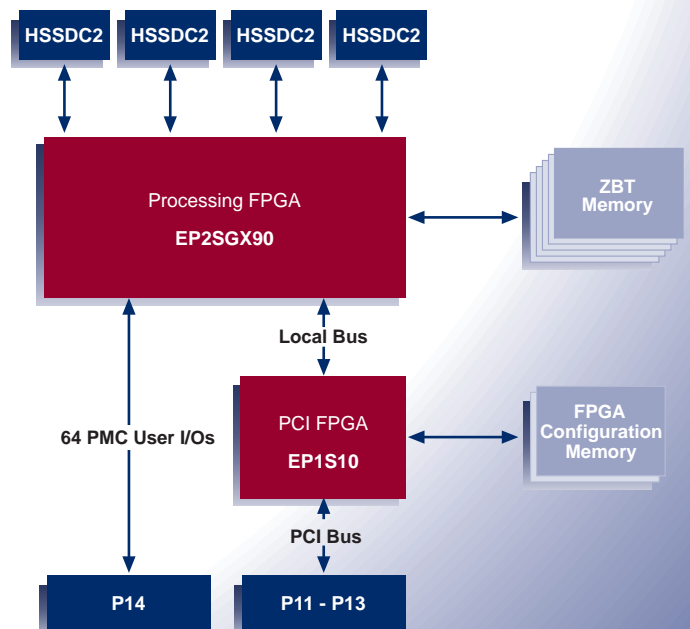
The **PM432** is a single PMC module that leverages on ALTERA® Stratix® II GX FPGA technology to provide a high-speed, high-bandwidth processing platform, ideally suited for Software Defined Radio (SDR), WiMAX, Radar, Video, as well as other computation and bandwidth intensive applications.

An EP2SGX90 Stratix II GX FPGA implements a processing node with an unprecedented combination of serial I/O bandwidth, logic and memory resources and DSP performance. Four Stratix II GX transceiver channels each provide up to 3.125 Gbps full-duplex bandwidth via HSSDC2 front panel connectors.

Five 512Kx36 (18Mb) ZBT® memories individually connect to the Processing FPGA, yielding 2.66 GBytes/sec of memory bandwidth.

An ALTERA EP1S10 Stratix FPGA implements a PCI-to-Local-Bus bridge with a 64-bit 66MHz PCI bus interface, supporting maximum PCI bandwidth to and from the Processing FPGA via separate 64-bit Target and DMA busses. From Pn4, 64 PMC user I/Os connect to the Processing FPGA.

The EP2SGX90 configuration data is stored in on-board flash memory that is programmable via the PCI bus.



Features

Processing FPGA

- EP2SGX90 ALTERA® Stratix® II GX FPGA
- 90,960 Logic Elements, 192 18x18 multipliers and 4.3 Mb RAM
- On-board non-volatile storage of configuration data (2 banks)
- Automatic configuration of FPGAs after power-up

Memory

- Standard: Five 512Kx36 (18Mb) ZBT® memories
- Optional: Five 1Mx36 (36Mb) ZBT® memories

PCI Interface

- 32/64-bit 33/66MHz 3.3V PCI bus in ALTERA® Stratix® FPGA
- Peak PCI data rate (533MBytes/s) supported
- Up to 420 MBytes/s sustained DMA data rate

PMC User I/O

- 64 User I/Os with LVTTTL signal level (3.3V)

Front Panel I/O

- Four HSSDC2 connectors
- Up to 3.125 Gbps full-duplex bandwidth per connector
- Serial RapidIO™, Fibre Channel, Gigabit Ethernet and SerialLite II protocols are supported via the use of IP cores

Software Support

- Software utility to program Processing FPGA configuration data
- Device driver for Windows 2000/XP and Linux
- Sample application and source code
- Matlab API via Mex DLL file available
- Application / driver development services available on request

Firmware Support

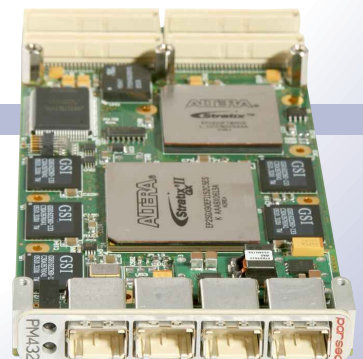
- Shipped with SerialLite II reference design
- FFT reference design available
- Firmware development services available on request

Typical Applications

- Software Defined Radio (SDR)
- Radar processing (Doppler filter, Pulse compression, CFAR)
- Image processing (DCT, 1D/2D convolution, etc.)
- Vector processing
- Real-time DSP functions (DDC, FFT, FIR, NCO, etc.)

Ordering Information

PM432 - Y - Z
Y: ZBT Memory Size (18Mb or 36Mb)
Z: HSSDC2 polarity (IN or FC)
(IN=Infiniband, FC=Fibre Channel)
(Standard order code: PM432-18-FC)



OUR *Purpose*

to enhance the
competiveness
of our clients

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